

WHAT IS CLAIMED IS

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1. A thin-film circuit substrate,
comprising:

10 a semiconductor substrate having a first
principal plane and a second principal plane that
counters the first principal plane,
a first insulator layer formed on the
first principal plane of the semiconductor substrate,
a through hole that continuously extends
15 from the second principal plane to the first
principal plane through the inside the semiconductor
substrate, including a main section substantially
having a first diameter and extending from the
second principal plane, and a tapered section having
20 a second diameter that is larger than the first
diameter near the first principal plane,
a second insulator layer that covers a
side wall face of the through holes, and
a thin-film circuit formed on the first
insulator layer.

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2. The thin-film circuit substrate as
30 claimed in claim 1, wherein the first insulator
layer is provided with an opening formed by an inner
wall surface of the second insulator layer of the
through holes.

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6. The thin-film circuit substrate as claimed in claim 2, wherein an insulator layer pattern that has a diameter larger than the openings, corresponding to the through hole, is provided between the thin-film circuit and the first

insulator layer.

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7. The thin-film circuit substrate as claimed in claim 1, wherein a thickness of the second insulator layer is larger than a thickness of the first insulator layer.

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8. The thin-film circuit substrate as claimed in claim 1, wherein the through hole is filled with an electrically conductive material.

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9. The thin-film circuit substrate as claimed in claim 1, further comprising a ferroelectric film or a high dielectric film.

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10. The thin-film circuit substrate as claimed in claim 1, wherein the first insulator layer and the second insulator layer are an oxide film.

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11. A manufacturing method of a thin-film circuit substrate, comprising:

a step of forming an etching stop film on a first principal plane of a semiconductor substrate having the first principal plane and a second principal plane,

5 a step of forming a resist pattern that has a resist opening on the second principal plane of the semiconductor substrate,

10 a step of forming a hole through the semiconductor substrate corresponding to the resist opening by applying dry etching to the semiconductor substrate using the resist pattern as a mask such that the etching stop film is exposed in the through holes,

15 a step of forming an insulator layer on a side wall face of the through holes,

a step of forming a thin film circuit on the etching stop film, and

20 a step of forming an opening by removing the etching stop film at the through hole such that the thin film circuit is exposed.

25 12. The manufacturing method of the thin-film circuit substrate as claimed in claim 11, wherein the dry etching is further continued after the etching stop film is exposed such that an over-etching is performed.

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35 13. The manufacturing method of the thin-film circuit substrate as claimed in claim 12, wherein the step of forming the etching stop film includes a step of forming an insulation film

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17. A via formed substrate, comprising:
5 a supporting substrate having a first principal plane and a second principal plane that counters the first principal plane,
a through hole having a first diameter, extending from the second principal plane toward the
10 first principal plane through the supporting substrate,
a taper form section that is formed in an edge section on the first principal plane side of the through holes, having an opening in the first
15 principal plane, with a diameter increasing from the first diameter toward the first principal plane until the diameter measured at the first principal plane reaches a second diameter that is larger than the first diameter,
20 a plug that is electrically conductive for filling the through holes, and
an electrode pad having a taper form corresponding to the taper form section, electrically connected to the plug.

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18. The via formed substrate as claimed in
30 claim 17, further comprising a vamp electrode on the electrode pad.

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19. The via formed substrate as claimed in claim 17, wherein the supporting substrate is made

of Si.

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20. The via formed substrate as claimed in claim 19, wherein the taper form section is formed on an Si crystal face.

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21. The via formed substrate as claimed in claim 17, wherein the second diameter is greater than twice as large as the first diameter.

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22. The via formed substrate as claimed in claim 17, wherein a thin-film circuit is formed on the supporting substrate.

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23. A manufacturing method of a via formed substrate, comprising:

a step of forming a tapered concavity by anisotropic etching on a first principal plane of a semiconductor substrate,

a step of forming an insulation layer in a form corresponding to the tapered concavity, covering the surface of the tapered concavity,

a step of forming such that a via hole that extends from a second principal plane that counters the first principal plane toward the first

principal plane of the semiconductor substrate
exposes the insulation layer at the tapered
concavity corresponding to the tapered concavity,

5 a step of forming an electrode pad on the
insulation layer that cover the tapered concavity in
a shape corresponding to a top part of the tapered
concavity,

10 a step of removing the insulator layer at
a bottom part of the via hole such that the
electrode pad is exposed, and

a step of forming a via plug by filling
the via hole with an electrically conductive
material.

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24. The manufacturing method of the via
formed substrate as claimed in claim 23, wherein the
20 semiconductor substrate is made of Si, and the
anisotropic etching process is performed by wet
etching.

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25. The manufacturing method of the via
formed substrate as claimed in claim 23, wherein the
via hole is formed by dry etching.

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26. The manufacturing method of the via
35 formed substrate as claimed in claim 23, wherein the
step of forming the via plug includes a plating
process of the electrically conductive material.

5 27. The manufacturing method of the via
formed substrate as claimed in claim 23, wherein the
electrically conductive material is one of Pt and Au.

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28. The manufacturing method of the via
formed substrate as claimed in claim 23, further
comprising:

15 a step of forming soldering paste on the
electrode pad, and
a step of preparing a solder ball on the
soldering paste corresponding to the electrode pad.

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29. The manufacturing method of the via
formed substrate as claimed in claim 28, further
25 comprising a step of forming a vamp electrode on the
electrode pad by applying heat to the solder ball.

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